CLAIMS

1. (Currently amended) A semiconductor device comprising a device forming area formed on a semiconductor substrate and a dicing line area arranged surrounding the device forming area, wherein

said dicing line area comprises first and second registration marks formed in different shots in respective registration mark areas,

a boundary line separates said respective registration mark areas, said boundary line defining a protruded portion and a recessed portion, respectively, at opposite directions on either side of the boundary line in a plane parallel to the substrate, the protruded portion containing at least one of the registration marks, and

said first and second registration marks each include an auxiliary mark to identify the first and second registration marks.

2. (Previously presented) The semiconductor device according to claim 1, wherein a surface of the semiconductor substrate is divided into a plurality of areas for performing photolithography process on each of the areas, each said area including either said first or second registration mark at an outermost peripheral portion, wherein

said auxiliary mark is an in-area position indication mark indicating relative position of respective ones of said first and second registration marks in said area.

3. (Original) The semiconductor device according to claim 2, wherein said first or second registration mark is formed in at least one of four corners of said area.

4. (Original) The semiconductor device according to claim 1, wherein said auxiliary mark has an arrow-like planar shape.

5. (Withdrawn) A semiconductor device including a device forming area formed on a semiconductor substrate and a dicing line area arranged surrounding the device forming area, wherein

a testing element area is formed in said dicing line area and said testing element area includes at least one selected from the group consisting of an identification mark identifying type of an electrode included in said testing element area, a position indication mark indicating a position of a contact hole formed in an interlayer insulating film arranged in said testing element area, a pitch correcting mark consisting of a plurality of line patterns spaced from and parallel to each other arranged in said testing element area, and a condition indication mark indicating a process condition arranged in said testing element area.

6. (Withdrawn) The semiconductor device according to claim 5, wherein said identification mark is formed on said electrode.

7. (Withdrawn) The semiconductor device according to claim 5, wherein planar shape of said identification mark forms a character, and a width of a line constituting said character is at most 10 μm.

8. (Withdrawn) The semiconductor device according to claim 5, wherein width of said identification mark is at least 30 μm.

9. (Withdrawn) The semiconductor device according to claim 5, wherein said position indication mark is an opening formed in said interlayer insulating film.

10. (Withdrawn) The semiconductor device according to claim 9, wherein planar shape of said opening is an arrow indicating direction of said contact hole.

11. (Withdrawn) The semiconductor device according to claim 5, wherein said testing element area further includes a conductive film formed on the dicing line area, and

said pitch correcting mark is positioned space from and adjacent to said conductive film.

12. (Withdrawn) The semiconductor device according to claim 5, wherein planar shape of said condition indication mark is a character representing a process condition.

13. (Withdrawn) The semiconductor device according to claim 12, wherein said process condition includes at least two selected from the group consisting of design dimension, on-mask dimension, resist target dimension and finished target dimension.

14. (Withdrawn) A photomask, comprising:

an area including a device pattern forming area and having rectangular planar shape;

a first outer peripheral dicing area in contact with one of a paired sides of the rectangle of said area and having a wide projected portion and a narrow recessed portion;

a second outer peripheral dicing area arranged in contact with the other one of said paired sides and having a recessed portion and a projected portion that fit said projected portion and said

recessed portion of said first outer peripheral dicing area, and registration mark areas arranged in said projected portions of said first and second outer peripheral dicing areas corresponding to four corners of the rectangle of said area; wherein

said registration mark areas include auxiliary mark areas indicating to which one of said four corners each mark corresponds.

15. (Withdrawn) A method of manufacturing a semiconductor device utilizing a method of exposure using the photomask according to claim 14.